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A Computer Model and Methodology to Predict Temperatures and Deformations during Diamond Multi-Wire Cutting

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Abstract. The Diamond wire slicing process for multi-Si wafering is relatively new, and there are limited three-dimensional thermal field simulations in this area. This work aims to fill the gap by using a Finite-Element model to simulate this complex mechanical-thermal process where the wires and wafers are continuously working in a thermally expanded region of the block. The non-uniform three-dimensional temperature field generated in the block leads to uneven contraction and deformation of wafers, which may impact on wafer strength. This process is not well understood. The model accounts for important slicing parameters such as cooling fluid flow rate, temperature difference, block length and wafer thickness in real production environment. It predicts a three-dimensional thermal field, and also quantifies wafer expansion/contraction at different places in a block. The obtained results can potentially help to optimize slicing recipe for better wafer strength and morphology, and to produce high quality wafers for solar panels.

INTRODUCTION

To manufacture a solar panel, a key step is to slice silicon blocks (multi/mono) into wafers. This process determines the strength of the wafers. The main influencing factors can be material wear mechanism, variation of temperature field and wafer deformation during slicing. Currently the mainstream for multi-Silicon wafering is the Slurry Slicing (SS) process [1-3]. It uses a mixture of oil and silicon carbide particles to saw silicon blocks into wafers through three-body-wear mechanism. Another technology, which is widely used for mono-Si wafering and currently undergoes fast development in multi-Si wafering, is Diamond Wire (DW) slicing [4-5]. In this process, wires with fixed abrasive (diamond particles) are used to saw the block into wafers through two-body-wear mechanism. Compared with SS process, DW slicing greatly reduces cutting time, wire consumption, and kerf loss.

The purpose of our work was to establish a three-dimensional Finite-Element model to examine influence of temperature field, deformations and thermal strains during the DW slicing process. In this process, large amount of heat is generated in the cutting zone (contact region of wire and block/wafer) with the result that the temperature in this region is increased. The wires and wafers are continuously working in a thermally expanded region of the block. As the emerging wafers cools down, they unavoidably contract. The non-uniform three-dimensional temperature field generated in the block leads to uneven contraction and deformation of the wafers, which may impact on wafer strength. This process is not well understood and a limited number of three-dimensional simulations in this area are reported. This work aims to fill this gap by simulation of the thermal condition inside the block, and to enable better understanding of wafer deformation and strength.

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THE MULTI-WIRE SLICING PROCESS

Figure 1 shows a typical diamond wire slicing setup where silicon bricks are sliced into wafers. Two short-length blocks were loaded in each saw run. A top plate was glued to the blocks and pushed downwards against the wire web. Each block had the dimensions 256 mm x 156.75 mm x 156.75 mm and was sliced into 882 wafers. After a forward motion of 600 m, the pilgrim direction was reversed and continued backward 560 m. This cycle was continuously repeated for about 2.5 hours till the slicing was completed. The velocity of the wires was 30 m/s. The wafering process was performed on a Meyer Burger multi-wire saw.

Coolant water was sprayed out from nozzles on two sides to the long vertical surfaces of the bricks, to transfer away the heat generated in the cutting zone (contact region). The total flow rate of water was 135 l/min, and the inlet and outlet temperatures were recorded to be 15.5 °C and 20.5 °C respectively. These data were used to estimate the amount of heat generated by the wires at the wire-silicon contact surfaces and absorbed by the silicon block. An internal cooling loop of the cutting fluid kept the lubricant at a constant temperature of 20 °C.

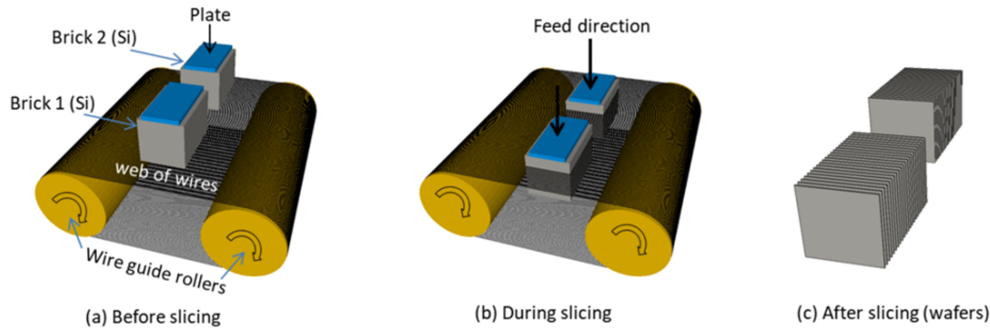

FIGURE 1. Slicing of two silicon blocks into wafers.

THE COMPUTER MODEL

Heat is generated at the contact interfaces between the moving diamond wires and the silicon block. Because of efficient external cooling, the silicon region adjacent to the wires has higher temperature than the rest of the block. As the wires moves upwards in the material, heat is continuously generated in the cutting zone, and is transferred to the other regions in the block, as well as to the cooling fluid. Meanwhile, the emerging wafers below the wires contract as they are quickly cooled down by the coolant flow. This transient temperature variation cause wafer expansion and contraction. The amount of contraction at a given location on each wafer corresponds to the temperature of the block when material was sliced at that location.

Despite its important part of the process to manufacture wafers, not least the great potential for cost reduction, a limited number of computer models that considers slicing of silicon blocks have been reported. Examples of such models are those of Johnsen [6] and Bhagavat [3,7], both considering slurry wafering based on silicon carbide as abrasive particles.

A key parameter for modelling the expansion/contraction of the silicon wafers during slicing is the heat generation between the wires and the block. For slurry wafering based on silicon carbide as abrasive particles, Johnsen [6] considered a constant heat generation of 0.18 W/mm. An approach accounting for the tension in the wires, wire velocity and wire bowing was applied by Bhagavat [7]. In our work the generated heat at the wire-silicon contact surfaces was based on measured flow rate, inlet and outlet temperatures of the cooling water;

$$P = \dot{m}\, c_P (T_{in} - T_{out}) \cdot \frac{\Delta s_W + \Delta s_K}{L} \cdot \frac{1}{N} \tag{1}$$

In Eq. (1) $\dot{m}$ is the mass flow rate of water, c_P is the specific heat of water, T_{in} is the inlet water temperature, T_{out} is the outlet water temperature, L is the length of the block, Δs_W is the wafer thickness (200 μm), Δs_K is the kerf or thickness (90 μm) of material that is removed by each wire and N is number of blocks loaded in each saw run. Based on Eq. (1) the heat generation at each wire-silicon contact surface was then calculated to be 53.4 W or 0.34

W/mm. This value is approximately twice the value applied by Johnsen [6] who did not consider diamond wire-saw cutting, but abrasive slurry cutting based on SiC particles. Those two methods to cut silicon blocks into wafers are very different in that the diamond wire sawing is a scratching-indenting process while abrasive slurry cutting is a rolling-indenting process.

The core diameter of the wires is 70 μm and each creates a kerf loss of 90 μm between the wafers. We assume that the effective diameter of the wires is equal to the gap thickness and that the upper half of this diameter constitutes the contact zone between the wire and the silicon. In addition, instead of rounded, this interface is approximated to be rectangular-shaped like shown in the RHS of Fig. 2. The total width of the heated contact surface, indicated by the red arrows in the figure, was then $\pi \cdot 90/2$ μm.

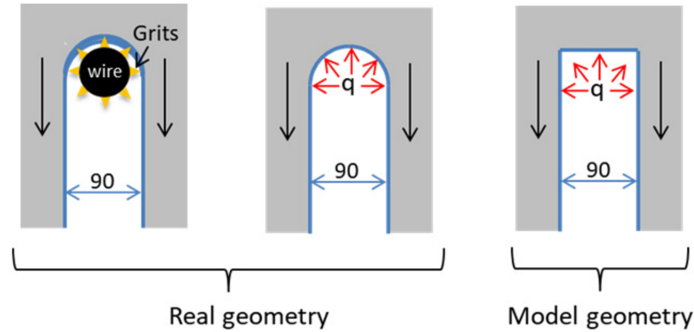

FIGURE 2. Simplification of the wire-silicon contact surfaces.

Because of the small dimensions of the block and the efficient water-cooling of the external surfaces, end effects cannot be neglected, which means that the model must be able to account for a three-dimensional temperature field. Combined with a large number of wafers emerging from the block, the ratio of the wafer width (or height) to the wafer thickness – which was 784 – easily creates a computational domain with a huge number of cells. Because of the symmetrical cooling condition, only a quarter of the block was modelled. If heating of the wires from the inlet side to the opposite outlet side was to be accounted for, the model should be expanded to include half the block. During the slicing, some of the coolant water is transferred into the center of the block where it cools both the contact surfaces and the wires. However, heating of the wires was not considered in the study. If experimental data becomes available and these prove that there is a significant temperature increase in the wires from the block entrance to the block exit, this effect should be accounted for in a future work. A wire speed of 30 m/s means that the contact time between a wire-cross section and the block is short and equal to approximately 0.005 sec. The number of cells included in the model was a compromise between computational time and accuracy.

Because material is successively removed as the wires progress upwards, the computational domain will change. The time to complete slicing of a block was approximately 2.5 hours, which means that the block slicing velocity was 0.0174 mm/s. Thermal conductivity in silicon is high. Compared to the slicing velocity, the conduction of heat flow in the block is significantly faster. Thus, a quasi thermal steady-state condition can be assumed to exist in the block. By building five stand-alone computational domains that represent the block when the wires have sliced 10%, 30%, 50%, 70% and 90% of the block height, the time-dependent temperature field was calculated.

THE GOVERNING EQUATIONS

Thermo-mechanical calculations were performed with the SiSim software [8], a finite element modeling tool that for this specific problem solves temperatures, deformations and strains in the block. Temperatures were solved according to the energy equation, i.e.

$$\rho \cdot c_p \frac{\partial T}{\partial t} = \frac{\partial}{\partial x_i}\left(\lambda \frac{\partial T}{\partial x_i} \right) + Q \tag{2}$$

where ρ is the density, c_p is the specific heat capacity, λ is the thermal conductivity and Q is a heat source term that accounts for heat generation caused by the work of the diamond-coated wires. Strains and deformations are unavoidable and appear due to thermal contractions in the materials. These are caused by heating/cooling and

temperature-dependent densities. Calculation of stresses was based on Cauchy's equilibrium equation;

$$\frac{\partial \sigma_{ij}}{\partial x_j} = \rho g_i \tag{3}$$

In this equation, the stress tensor σ_{ij} represents component *i* of the force per unit surface with normal direction *j* and g_i is the gravitational acceleration. Because of the relatively low temperatures in the silicon block, only thermal strains were considered. The material properties in both Eq. (2) and (3) depend on the temperature.

Without other details about the water spray-cooling than the flow rate and the inlet/outlet temperatures, an estimate of the heat-transfer coefficient on the external surfaces of the silicon blocks is challenging. However, cooling by means of a water spray is known to be efficient and promote high cooling of the block. A heat-transfer coefficient equal to 10000 W/(m^2·K) was applied on all external sides except the block bottom side. A heat-transfer coefficient was also specified for the emerging wafer surfaces which are separated by a gap of 90 µm. A mixture of 2% lubricant and 98% water cool these surfaces, and the local heat transfer coefficient is likely to vary both with the position inside the gap and with the position of the wires. Knowledge about the detailed entrainment of water into the groove was not available, and for simplicity a constant heat-transfer coefficient equal to 10 W/(m^2·K) was employed in our study. It's a rather low value that assumes that interior wafer surfaces are not covered by a continuous water film.

A force that corresponds to a weight of 30 kg was specified at the block top surface. At the wire contact surfaces a distributed spring stiffness that displaced these 1 mm downwards were applied as mechanical boundary condition. Zero normal displacement was specified as mechanical boundary condition for the two symmetry surfaces. All other surfaces were free to move, also the emerging wafer surfaces in the block.

RESULTS

At the time when half the block was sliced into wafers (50% as defined above), the resulting temperatures are shown in the RHS of Fig. 3. The thermal field is highly three-dimensional with the core of the block exhibiting the highest temperatures. The maximum temperature increase is 139 °C. This is significantly higher than the value calculated by Johnsen [6], which was 35 °C. However, they were examining abrasive slurry wire cutting of an air-cooled block with a heat flux of 0.18 W/mm applied at the wire-silicon interface, approximately half the value applied in our study, but with a significantly longer slicing time of 4.3 hours. Applying their heat flux at the contact surfaces would reduce the maximum temperature increase from 139 °C to 62 °C in the simulation. Our model of the heat transfer between the diamond wires and the silicon contact surfaces is based on measured water flow rate and increase of cooling-water temperature and, because the time to complete the sawing is long and the heat conduction in the block is large, it is believed to reflect the actual heat that is absorbed by the silicon block.

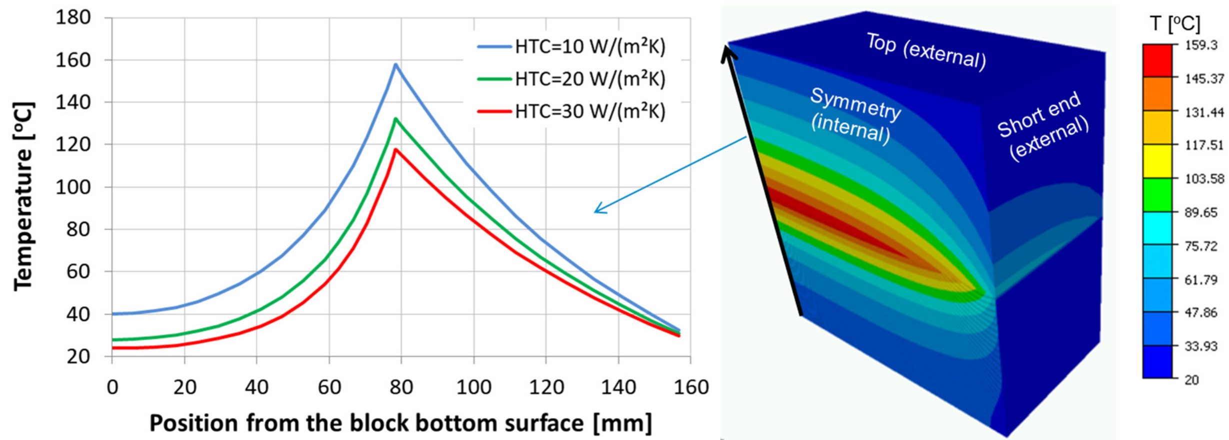

FIGURE 3. Temperatures after half the block has been sliced by the diamond-coated wires.

Also displayed in Fig. 3 is the vertical temperature profile that runs from the bottom to the top along the center of the block. Three curves based on different values for the heat transfer coefficient applied on the emerging wafer surfaces in the grooves are included. While 10 W/(m^2·K) represents the chosen value, the other two – 20 W/(m^2·K) and 30 W/(m^2·K) – indicate the sensitivity and the influence of improved cooling. For a heat transfer coefficient equal to 20 W/(m^2·K), the maximum temperature in the block decreases from 159 °C to 133 °C. A further increase to 30 W/(m^2·K) makes the same temperature drop to 117 °C.

Figure 4 shows the development of the temperature field in the block as a function of the vertical position of the diamond coated wires. Each figure represents a stand-alone computation, but because of the long cutting time and the large thermal conductivity of silicon, these have been combined and approximated to represent the time-dependent temperature field in the block during slicing. The percentage value added to each figure indicates the position of the wires relative to the block height. The maximum temperature was always obtained at the cutting zone. Because of the poor cooling of the bottom surface, the maximum temperature was larger in the first part of the slicing. What is obvious from Fig. 4 is that the wires are successively removing material in a part of the block that has increased temperature and, because of thermal expansion, the wafers will contract as they cool down. Because the temperatures are not uniform, the expansion-contraction will vary in the emerging wafers. As the wires work their way upward through the block, the calculations show that the maximum temperature drops. Represented by a similar vertical temperature profile as in Fig. 3, corresponding vertical temperature profiles for different wire positions are included in the bottom right part of Fig. 4.

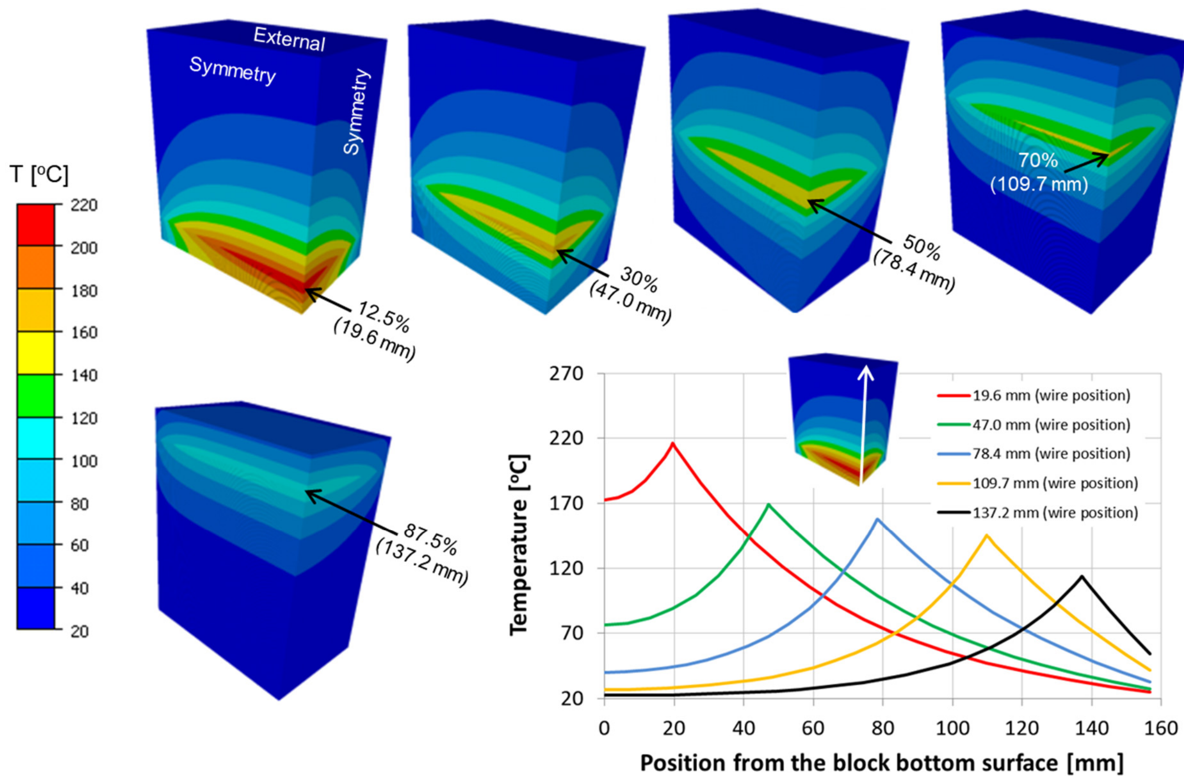

FIGURE 4. Temperatures during the slicing of the silicon block.

Calculated thermal strains after the wires have sliced half the block is shown in the LHS of Fig. 5. These compare well with the temperature field in Fig. 3. The maximum thermal strain follows the front of the wires in the center of the block, and is a magnitude of order 10^{-4}. These are calculated as the product of thermal expansion and the temperature increase, i.e.

$$\varepsilon_T = \beta \cdot (T - T_0) \tag{4}$$

where T_0 is the initial temperature (20 °C) and T is the calculated temperature. As a result, the time-dependent field of the thermal expansion has similar shape as that for the temperature. There is some dependency of the thermal expansion coefficient to the temperature, which increases from $\beta = 2.9 \cdot 10^{-6}$ at 20 °C to $\beta = 3.5 \cdot 10^{-6}$ at 220 °C. The curve included in the RHS of Fig. 5 shows the maximum thermal strain as a function of the vertical position of the wires above the block bottom surface. As the temperatures drop with the time (height), so do the thermal strains induced in the block.

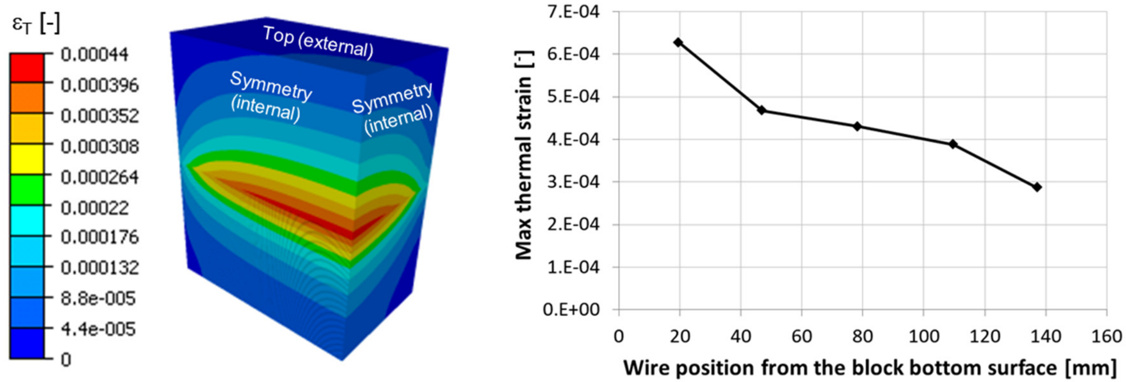

FIGURE 5. Thermal strains after half the block has been sliced by the multi-wires.

Horizontal displacements in the x-direction, i.e. in a direction normal to the wafer surfaces, as a function of the wire position, shown as a percentage of the block height, are displayed in Fig. 6. The orientation of the displayed block is such that only the external surfaces of the quarter block are visible. Two comments should be made on the contour plots in this figure. First, they reveal that the deformations increase with the time or the vertical position of the wires. Second, they show that the deformations increase with the distance away from the symmetry planes. When the wires have completed 87.5% of the block, the deformations on the external short side vary linearly from 214 μm at the bottom to 8 μm at the top.

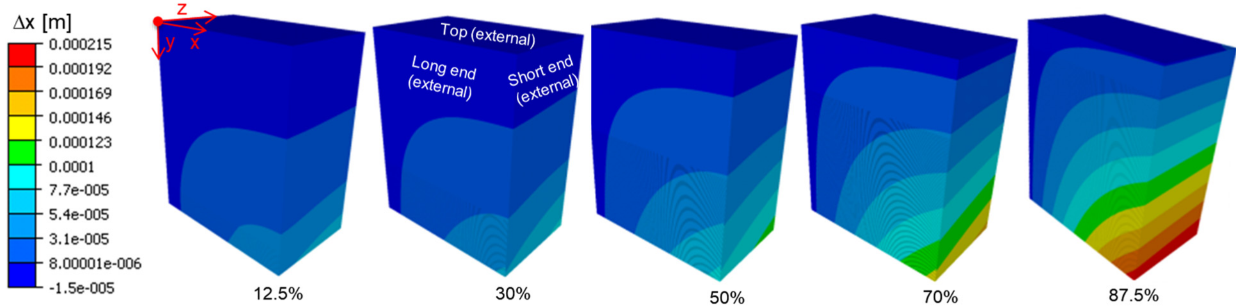

FIGURE 6. Deformation of the block during the slicing.

More details on the displacements in a direction normal to the wafer surfaces are shown in Fig. 7, which shows the situation when the wires have sliced half the height of the block. In this picture the deformations in the block have been magnified by a factor 500. The symmetry surface is locked, but for numerical reasons it has obtained a small but insignificant negative displacement. The wafers emerging from the block are free to move. In general, the wafer area near the cutting zone subjects to larger displacements than the solid above the wires. In their examination of wafers sliced by diamond-coated wires, Chen [9] measured saw marks with typical height equal to 5 μm on the wafer surfaces. In our simulations, the deviation from the wafer nominal thickness (200 μm) due to contraction was significantly less and of the order 10^{-2} μm. This contraction can be estimated from the product of the wafer thickness and ε_T where the latter is calculated from Eq. (4).

Bowing of the wafers can be derived from the results of the thermo-mechanical calculations. Because the wires are continuously working in a heated and expanded region of the block, these will not cut the block in the same position as if the block was cold. Displacements normal to the wafer surface are zero at the symmetry plane and

largest at the block short end surfaces, as shown on the RHS of Fig. 8. This part of the figure also identifies three positions at the short end – A, B and C – that are located at the same vertical height as the wires and that follow the wires upwards in the block. Initially the block is cold, and the wires start to cut when there are no displacements present. When the wires have sawn 12.5% (19.6 mm) of the block height, the displacements normal to the wafer surfaces at the wire height position on the block short end are seen to increase rapidly to 39-49 µm. From this height to 137 mm (87.5% of the block height), these displacements slowly decrease. Bowing of the wafers is found to be largest for the wafers closest to the block short ends, smallest for those at and adjacent to the symmetry plane. Along the short-end wafer height, the calculations suggest that the maximum wafer deflection is 49 µm (maximum value of A, B and C). The simulations also suggest that there will be deflection of the wafer along the width of the wafer, and the maximum value, again appearing at the block ends, is the difference between the value in position A and C. The maximum deflection in this direction was then calculated to be 10 µm.

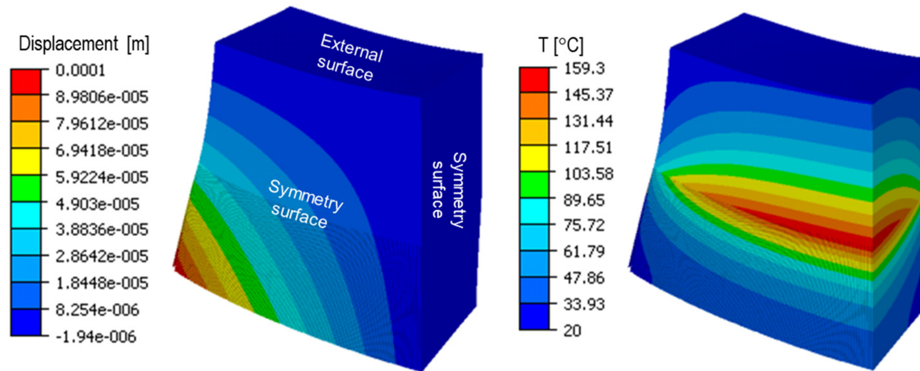

FIGURE 7. Deformations, magnified by a factor 500, and temperatures in the block during multi-wire slicing.

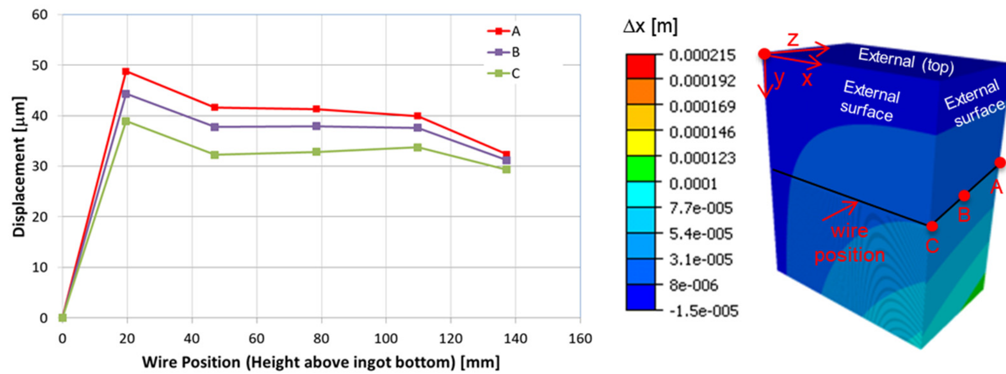

FIGURE 8. Displacements (normal to the wafer surface) of the block short end at the position of the multi-wires.

A parameter study was carried out to examine the influence of changed heat generation between the wires and the silicon block contact surfaces. In the study, Eq. (1) was used to determine this value to be 0.34 W/mm. Calculations were first performed with the inlet water temperature reduced from 15.5 °C to 14.5 °C and the outlet water temperature unchanged to account for increased cooling, or alternatively, keeping the inlet water temperature unchanged and increasing the water flow rate by 20%. This corresponds to a heat generation of 0.28 W/mm between the wires and the silicon block. Similar computations were completed with the inlet water temperature increased by 1.0 °C to account for reduced cooling. This corresponds to a heat generation of 0.43 W/mm between the wires and the silicon block. Results that both display the maximum temperature and the maximum thermal strain in the block as function of the position of the wires and the contact surface heat generation are included in Fig. 9. When the wires were halfway through the block, an increased heat generation of 0.43 W/mm caused the maximum temperature in the silicon to increase by 34.4 °C. A similar reduced heat generation to 0.28 W/mm caused the maximum temperature to decrease by 31.9 °C, i.e. from 158.2 °C to 126.3 °C. Near the bottom the maximum thermal strains

are within ± 28% of the value based on a heat generation 0.34 W/mm, near the top the differences are reduced to be within ± 23%.

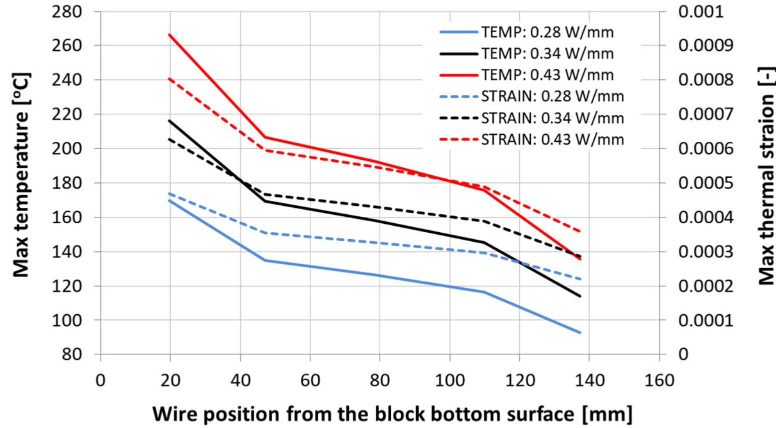

FIGURE 9. Maximum temperature and corresponding thermal strain in the block with changed cooling conditions.

DISCUSSION

A wafer thickness of 200 µm was considered in this study. While the preferred thickness of mc-Si produced today is 180 µm, the trend predicts, according to the International Technology Roadmap for Photovoltaic (ITRPV) [10], a further thickness reduction to 150 µm in 2027. For mono-Siicon the similar trend forecast is thickness reduction to 140 µm. For the block size that was considered in this study and unchanged wire diameter, thinner wafers means that a larger number of wires are required to do the slicing. If the generated heat at the wire-silicon contact surfaces remains unchanged at 0.34 W/mm and the wafer thickness is reduced to 100 µm, simulations show generally higher temperatures in the block during the slicing. Detailed results are not shown here, only briefly commented. At the time when the wires were halfway through the block, which correspond to the block and wire positions shown in Fig. 3, the temperatures were 14.0 °C to 90.8 °C higher in the plane of the wires and 0.4 °C to 6.1 °C higher at the block top surface. At the bottom side the temperatures were up to 6.8 °C colder. Otherwise the shape of the temperature field was similar. The fact that the temperature variations in the block were larger gave a maximum thermal strain that was 72% larger than for case study based on wafer thickness of 200 µm.

Wafer strength has not been commented on. Appearance of multiple parallel saw marks (grooves) on the wafer surface is a well-known defect caused by DW slicing. A method to characterize the strength of a wafer is to use the four-point bending test where the force and the deflection are increased until breakage of the wafer. Smallest maximum deflection and force is obtained when the bars were parallel to the saw marks (weak direction), largest when they were perpendicular (strong direction). To examine the influence of slower slicing speed and use of smaller grit size, bending tests of as-cut wafers were compared to a wafer representative for the case study. The results are shown in Table 1. By slowing the downward table feed of the sawing tool, the cycle time was increased by 30%. The influence of smaller grit size was examined by switching from grit sizes in the range 4.7 µm to 9.3 µm on the diamond wire to the range 3.9 µm to 7.8 µm. While the results show a significant difference of the breaking force in the weak and the strong direction, slowing the feed speed or reducing the grit size did not have much impact on the wafer strength.

TABLE 1. Results of the four-point bending test to characterize the wafer strength. Wt = wafer thickness, R_a = surface roughness, F_B = breaking force, s_B = maximum wafer deformation/deflection.

	Wt [µm]	R_a [µm]	F_B [N] Strong	F_B [N] Weak	s_B [mm] Strong	s_B [mm] Weak
This study (base)	196.82	0.17	11.37	5.40	10.75	5.84
Slower feed speed	194.52	0.17	12.71	5.31	12.94	5.71
Smaller grit sizes	197.70	0.14	10.74	5.56	10.95	5.67

CONCLUSIONS

In the diamond wire slicing process, the block and the wafers were subject to a transient temperature field. A large amount of heat was continuously generated in the cutting zone and quickly transferred to other regions of the block, and to the cooling fluid. This transient temperature field leads to un-even thermal strain and stress in block, as well as wafer expansion/contraction. Since the diamond wire slicing process for multi-Si wafering is relatively new, and there are limited three-dimensional thermal field simulations in this area, this work aims to fill the gap by using a 3D Finite-Element solver to simulate this complex mechanical-thermal process. The current model is able to take into account important slicing parameters such as cooling fluid flow rate, temperature difference, block length and wafer thickness in real production environment. It predicts a three-dimensional thermal field, and also quantifies wafer expansion/contraction at different places in a block. The obtained results can potentially help to optimize slicing recipe for better wafer strength and morphology, and to produce high quality wafers for solar panels.

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